LISTING OF THE CLAIMS

Please amend the claims as shown below. Claims 8-9, 16, 20-27, and 29-30 are amended herein. Please cancel Claims 6-7, 14-15, 17-19 and 28 without prejudice. No new matter is added. This listing of claims will replace all prior versions and listings of claims in the Application.

1-7. (Cancelled)

8. (Currently Amended) ~~The semiconductor structure as recited in Claim 7 wherein said resistive value of said resistance is fixed with setting a particular number for said portion of said plurality of individual vias in parallel~~ A semiconductor structure comprising:

a pad area;

an electrostatic discharge protective device disposed directly below said pad area, said electrostatic discharge protective device comprising a transistor and a resistance, wherein said pad area comprises:

a substrate;

a first layer of metal disposed above said substrate wherein said electrostatic discharge protective device is disposed below said first layer of metal; and

a second layer of metal disposed above said first layer of metal;

a layer of dielectric disposed between said first metal layer and said second metal layer; and

a via disposed within said dielectric layer wherein said via electrically couples said first and said second metal layer, wherein said via comprises a plurality of individual vias, wherein said resistance comprises a portion of said plurality of individual vias, wherein said individual vias comprising said portion are arranged

electrically in parallel one to another and wherein a resistive value of said resistance is configurable during a process for fabricating said semiconductor structure, wherein said resistive value of said resistance is fixed therein with setting a particular number for said portion of said plurality of individual vias in parallel.

9. (Currently Amended) The semiconductor structure as recited in Claim 8 [[6]] further comprising a subsequent layer of metal between said first and said second metal layers.

10-15. (Cancelled)

16. (Currently Amended) ~~The pad area apparatus as recited in Claim 15 wherein said resistive value of said resistance is fixed with setting a particular number for said portion of said plurality of individual vias in parallel~~ A pad area apparatus for a semiconductor structure comprising:

a substrate;

a first layer of metal disposed above said substrate;

a second layer of metal disposed over said first layer of metal;

an electrostatic discharge protective device wherein said electrostatic discharge protective device is disposed within said substrate directly below said pad area and wherein said electrostatic discharge protective device comprises a transistor and a resistance;

a layer of dielectric disposed between said first metal layer and said second metal layer; and

a via disposed within said dielectric layer wherein said via electrically couples said first and said second metal layer, wherein said via comprises a plurality of individual vias, wherein said resistance comprises a portion of said plurality of

individual vias, wherein said individual vias comprising said portion are arranged electrically in parallel one to another and wherein a resistive value of said resistance is configurable during a process for fabricating said semiconductor structure, wherein said resistive value of said resistance is fixed therein with setting a particular number for said portion of said plurality of individual vias in parallel.

17-19. (Cancelled)

20. (Currently Amended) ~~The electrostatic discharge protective device as recited in Claim 19 wherein said resistive value of said resistance is fixed with setting a particular number for said portion of said plurality of individual vias in parallel~~ An electrostatic discharge protective device for a semiconductor structure comprising:

a resistance; and

a transistor disposed within a substrate directly below a pad area of said semiconductor structure, wherein said resistance comprises a plurality of vias of said semiconductor structure, wherein said vias are arranged electrically in parallel, one to another, and wherein a resistive value of said resistance is configurable during a process for fabricating said semiconductor structure wherein said resistive value of said resistance is fixed with setting a particular number for said portion of said plurality of individual vias in parallel.

21. (Currently Amended) The electrostatic discharge protective device as recited in Claim ~~19~~ 20 wherein said resistive value of said resistance is fixed with forming said individual vias comprising said portion of said plurality of individual vias with a particular cross sectional area.

22. (Currently Amended) The electrostatic discharge protective device as recited in Claim ~~19~~ 20 wherein said resistive value of said resistance is fixed with forming said individual vias comprising said portion of said plurality of individual vias with a particular length.

23. (Currently Amended) The pad area apparatus as recited in Claim ~~15~~ 16 wherein said resistive value of said resistance is fixed with forming said individual vias comprising said portion of said plurality of individual vias with a particular cross sectional area.

24. (Currently Amended) The pad area apparatus as recited in Claim ~~15~~ 16 wherein said resistive value of said resistance is fixed with forming said individual vias comprising said portion of said plurality of individual vias with a particular length.

25. (Currently Amended) The semiconductor structure as recited in Claim [[7]] 8 wherein said resistive value of said resistance is fixed with forming said individual vias comprising said portion of said plurality of individual vias with a particular cross sectional area.

26. (Currently Amended) The semiconductor structure as recited in Claim [[7]] 8 wherein said resistive value of said resistance is fixed with forming said individual vias comprising said portion of said plurality of individual vias with a particular length.

27. (Currently Amended) A method of fabricating an semiconductor structure, comprising:

disposing a pad area upon a substrate;

disposing an electrostatic discharge protective device directly below said pad area, said electrostatic discharge protective device comprising a transistor and a resistance, wherein said pad area comprises:

a first layer of metal disposed above said substrate wherein said electrostatic discharge protective device is disposed below said first layer of metal; and

a second layer of metal disposed above said first layer of metal;

disposing a layer of dielectric between said first metal layer and said second metal layer; and

disposing a via within said dielectric layer wherein said via electrically couples said first and said second metal layer, wherein said via comprises a plurality of individual vias ~~and~~ wherein said resistance comprises a portion of said plurality of individual vias, wherein said individual vias comprising said portion are arranged electrically in parallel one to another and wherein said disposing a via comprises actively configuring a resistive value of said resistance, wherein said resistive value of said resistance is fixed therein with setting a particular number for said portion of said plurality of individual vias in parallel.

28. (Cancelled)

29. (Currently Amended) The method as recited in Claim 27 wherein [[a]] said resistive value of said resistance is further fixed with forming said individual vias comprising said portion of said plurality of individual vias with a particular cross sectional area.

30. (Currently Amended) The method as recited in Claim 27 wherein [[a]] said resistive value of said resistance is further fixed with forming said individual vias comprising said portion of said plurality of individual vias with a particular length.